REMARKS

This application has been carefully reviewed in light of the final Office Action dated July 5, 2005. Claims 1 to 18 are pending in the application. Claims 1, 11, 17 and 18 are in independent form. Reconsideration and further examination are respectfully requested.

Applicant thanks the Examiner for maintaining the indication of allowable subject matter in Claims 17 and 18.

Applicant also thanks the Examiner for maintaining the indication that Claims 9, 10, 13 and 14 would be allowable if rewritten in independent form, including all of the limitations of the base claims. Applicant has chosen not to rewrite these claims at this time, since the base claims for each of Claims 9, 10, 13 and 14 are believed to be allowable for at least the reasons set forth below.

In the Office Action, Claims 1 to 8, 11, 12, 15 and 16 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 5,357,152 (Jennings) in view of U.S. Patent No. 6,112,019 (Chamdani) and U.S. Patent No. 5,491,694 (Oliver). This rejection is respectfully traversed.

Referring specifically to the claims, independent Claim 1 is directed to a computer processor including a plurality of processing units. The computer processor also includes communication means including a common bus to which each of the plurality of processing units are interconnected for communication of packetized information over the common bus. In addition, the communication means is dynamically configurable based on a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units in at least first and second distinct

configurations, the first distinct configuration having a larger number of the processing units arranged in parallel than the second distinct configuration, and the second distinct configuration having a deeper pipeline depth than the first distinct configuration.

Independent Claim 11 is directed to a method of data processing using a computer processor having a plurality of processing units interconnected by a common bus forming at least part of communication means by which packetized information is communicated between the processing units. The method includes the step of dynamically configuring the communication means according to a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units in a plurality of configurations having a different number of the processing units arranged in parallel and a different number of the processing units arranged in pipelined layers.

A feature of the invention of Claims 1 and 11 therefore lies in a communication means including a common bus for communication of packetized information between processing units, wherein the communication means is dynamically configurable based on a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units. The applied references of Jennings, Chamdani and Oliver are not seen to disclose or suggest at least this feature.

The December 28, 2004 Office Action cited to Figure 2 of Jennings, and equated Jenning's programmable circuit and configurable signal bus LSF and LSC with the claimed communication means. In addition, the Office Action associated Jenning's logic networks with the claimed processing units.

At page 2 in the current Office Action, attention is now directed to Figure 5 and column 7, lines 55 to 68 of Jennings, for the alleged disclosure of communication means which are dynamically configurable. This cited portion of Jennings discloses that a logic network comprises three stages, each stage including two groups of programmable memory cell sets, two Universal Boolean Function Generators (UBFG), and an external port. Jennings further discloses that the programmable logic circuit provides signals via the LSF bus to the programmable memory cell sets, and that the UBFG performs logic functions based on the signals to the programmable memory cell sets. See Jennings, column 8, lines 40 to 58.

In other words, Jennings is seen to disclose that each logic network comprises three stages associated with performing a desired logic function. The programmable circuit and signal bus LSF of Jennings are seen to affect the performance of a function for a particular logic network. As such, Jennings is seen to correspond with a configurable arrangement of functions within one logic network. However, Jennings is not seen to disclose or suggest that its programmable circuit and configurable signal bus LSF are dynamically configurable between logic networks. In contrast, the communication means in the invention of Claims 1 and 11 is dynamically configurable for communication paths between processing units.

In Jennings, the functionality of a UBFG within a particular logic network is seen to be programmable via memory cell sets. However, Jennings is not seen to disclose or suggest that communication paths between the UBFGs themselves are configurable, muchless dynamically configurable. The abstract of Jennings further suggests configurability within, but not between logic networks, by disclosing "a logic system

comprising one or more logic networks that can perform a variety of preconfigured or preconfigurable logic functions".

Accordingly, Jennings is not seen to disclose or suggest at least the feature of a communication means including a common bus for communication of packetized information between processing units, wherein the communication means is dynamically configurable based on a processing of a computer program to thereby selectively arrange communication paths for the packetized information between the processing units.

In addition, Chamdani and Oliver have been reviewed and are not seen to compensate for the deficiencies of Jennings.

Accordingly, based on the foregoing amendments and remarks, independent Claims 1 and 11 are believed to be allowable over the applied references.

The other claims in the application are each dependent from the independent claims and are believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

No other matters being raised, it is believed that the entire application is fully in condition for allowance, and such action is courteously solicited.

Applicant's undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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